Unique Technique of Extraction/Insertion of E1 byte in SDH Network for Optical Voice Communication

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Abstract- Purpose of this paper is to describe the hardware and software design implementation of extraction or insertion of E1 byte for optical voice communication .This voice communication allows field engineers to communicate during installation, commissioning and maintenance of telecommunication networks. This protocol provides robust structure and shall operate with a minimum of resources even if parts of the network are out of service. This structure in telecommunication system is called Engineering Ordered Wire (EOW).

Index Terms- CODEC, DTMF, G.703, FPGA, ITU V.11, SDH, SLIC.

I. INTRODUCTION

The E1 and E2 byte in section overhead of SDH frame can be used for optical voice communication through optical fiber. This type of protocol can be used as telephone service with 64kbps channel between telecommunications sites. This is called DTMF-EOW (Dual Tone Multi Frequency–Engineering Order Wire) [1-4]. Installation, configuration or maintenance of equipment can be done by using DTMF EOW .Selective calling and group calling may be possible through EOW. The digital EOW signal is sent between modules via cables. The physical format here is ITU V.11 [5-9].The present author has described only the overview of EOW in [10] but here details description of each and every components are described vividly. EOW module can send or receive data through G.703 interface. Here the data is framed and transferred as per ITU-T recommendation G.703 (Physical/electrical characteristics of hierarchical digital interfaces) to make it compatible the G.703 interface output inserts fill bytes to make up its 64 Kbit/s or 8 Kbytes/s stream from the internal 7.877 Kbytes/s. The G.703 interface input removes fill bytes to get a nominal rate of 7.877 Kbytes/s into the receiver FIFO buffer. The main voice channel processing is done in FPGA with 7.877 kHz, 8 bits wide voice channel.

II. HARD WARE DESIGN DESCRIPTION

In FPGA all input signals are added to make up the out-put voice signals. The telephone is connected to a SLIC, sub-scriber line interface circuit, via a relay. The SLIC supplies 48V to the telephone and converts the 2-wire telephone signal to/from a 4-wire transmit and receive signal.

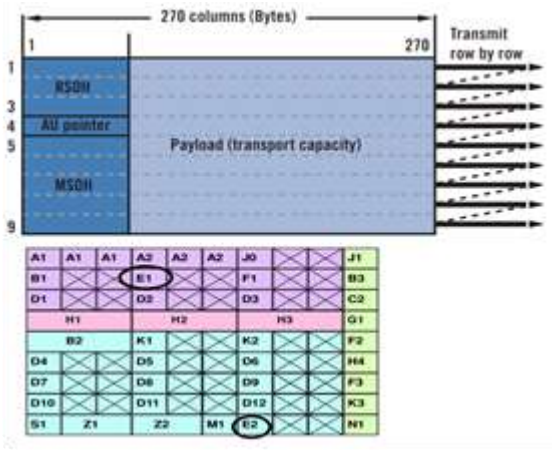

Fig. 1.STM-1 frame structure showing the position of E1 and E2 byte.

The relay is used to switch a ringing signal to the phone. The ringing signal and various other sine wave tones are generated from a programmable tone generator. The tone output can be added to the telephone signal in both transmit and receive directions. A DTMF, dual tone multi frequency, receiver is always connected to the EOW telephone. This DTMF receiver listens for commands from the EOW telephone. Another DTMF receiver is always connected to the audio signal output from the voice channel processing block. This DTMF receiver listens for commands from the EOW line. The voice signal processing clock frequency and other clock frequencies are derived from a common reference crystal oscillator with accuracy better than +/- 100 ppm.

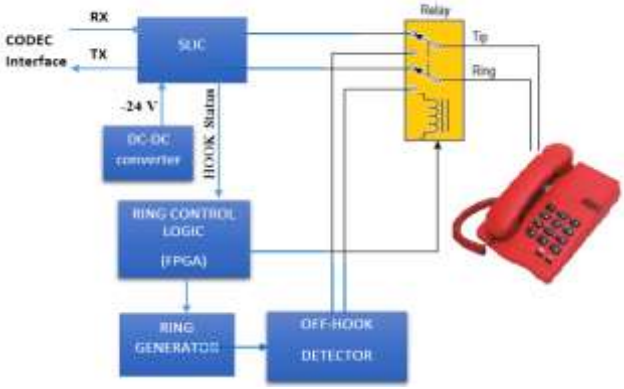

Fig. 2 .Schematic diagram of SLIC and Telephone Interface

A. Subscriber line Interface

The SLIC (Subscriber Line Interface Circuit) is used to connect the EOW phone set .The function of the SLIC is to supply the power to the telephone and also converter 2-wire to 4-wire transmit and receive signal. Various sine wave tones are generated by tone generator controlled by FPGA .These sine waves are added to the telephone signal in both transmit and receive operation.

The SLIC is AG1171 [11] by Silver Telecom. It is a ringing slic, i.e., with inbuilt DC-DC converter to generate ring voltage. SLIC operates at both 3.3V and at 5V. SLIC outputs a High condition on SHK signal during Off-Hook condition. FPGA controls the ring signals (F/R and RM) to SLIC. TIP and RING signals are interfaced to RJ11 jack to connect with a standard 600 ohm impedance telephone. The analog side is interfaced to CODEC. The schematic block diagram of SLIC and telephone line is shown in figure 2.

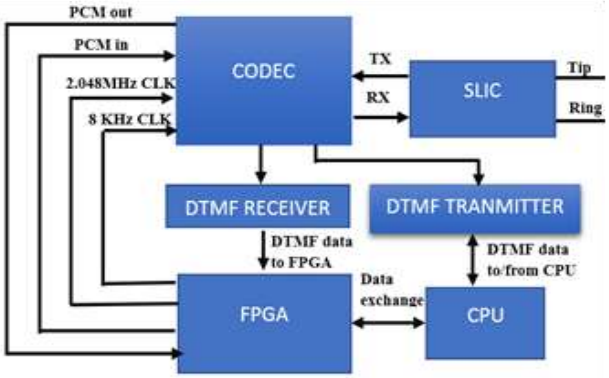

Fig. 3 .Schematic diagram of SLIC and CODEC Interface

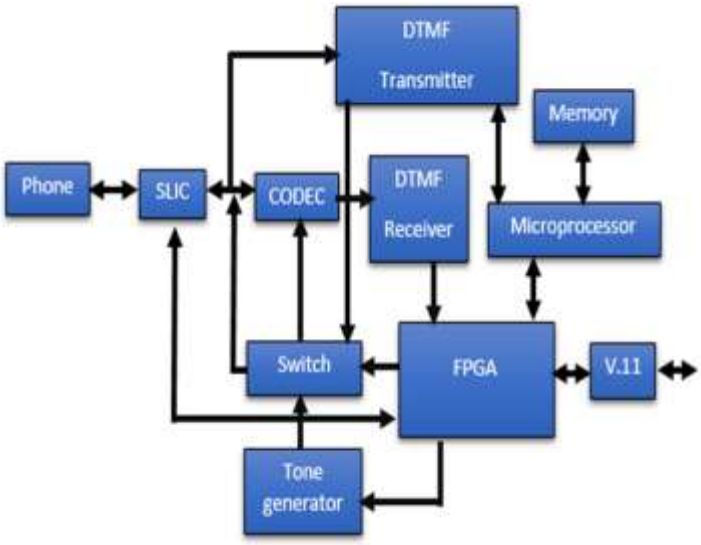

Fig. 4. Schematic diagram of the system including CPU, FPFA, CODEC and SLIC DTMF interfaces

Referring to the block diagram (Figure 2), in the standby state (phone on–hook, not ringing), the relay connects the phone line to the SLIC. When the phone is taken off–hook, the SLIC provides the loop current, and the speech paths between the phone and the CODEC. The HOOK STATUS output (from the SLIC) is provided to the FPGA. The dc–to–dc converter provides the –24 V (from the 5.0 V supply) necessary to power the SLIC and provide the loop current. When the phone is on–hook, and ringing is to be applied, the Ring Control Logic (controlled by the FPGA) powers the Ring Generator, and switches the relay so as to provide the ringing voltage to the phone line. The Off–Hook Detector informs the logic if the phone is taken off–hook during ringing. The Ring Control Logic then switches the relay to the SLIC.

B. CODEC

The CODEC provides the A/D and D/A conversions of the voice band signals between the digital system and the SLIC. AM79Q5457 [12] by Legerity is a 4-channel CODEC. Channel-1 is used for EOW phone and channel-4 is used for DTMF signaling. Transmit and receive frame signals are separate for all channels and is controlled by FPGA. Unused channels 2 & 3 will be power downed. PCM or digital side of CODEC is interfaced with FPGA. 8-bit sampling with A-law coding technique is used. The schematic block diagram of SLIC and CODEC is shown in figure 3.

C. FPGA

In this design FPGA plays vital role for mapping and de-mapping of E1 byte in STM1 frame. Mapping is the process of insertion of overhead and pointer information in payload for the generation of STM frame. A mapper perform the following functions: Insertion of path overhead in payload, insertion of AU pointers, and insertion of Regenerator section overhead bytes and multiplexer section overhead for formation of STM Frame. De-mapping is the process of extraction of overheads and stuff bits from STM frame, to obtain payload information. A de-mapper perform the following functions: Detect and align to the SDH framing pattern and synchronization and generate LOS, OOF and LOF alarms. Extract regenerator section overhead and multiplexer section overhead and detect errors. Process AU pointers, detect all the errors for VCs and extracts higher order path overhead. The process of mapping and de-mapping is done in FPGA by writing VHDL code and the code is converted to .bit file to download through JTAG connector.

D. SWITCH

For switching of DTMF tones and signaling tones, like Dial tone, busy tone, information tone etc., to EOW line and EOW phone side, analog switch is used. Switches are controlled from FPGA. "DG444" or CBTLV3125PWR will be used.

E. DTMF Receiver

MT8870DS DTMF receiver or MT88L70 can be used [13]. The DTMF receiver is always connected to listen to the embedded EOW line. The DTMF receiver outputs a "tone valid" signal. This signal goes to the FPGA where it can generate interrupt. The valid 4-bit DTMF code can be read by FPGA upon getting tone valid signal.

F. DTMF Transceiver

MT8888C DTMF transceiver or MT88L85 can be used [14]. The DTMF receiver in the transceiver is always connected to listen to the signal from the EOW phone. This makes it possible to receive commands from the EOW phone before opening for the EOW line. DTMF transceiver interrupts microcontroller [15] via FPGA [16] on receiving a valid DTMF tone from EOW phone. The decoded 4-bit DTMF value is directly read by microcontroller. The transmitter part is used to send DTMF signals while establishing a communication channel. The DTMF transmitter in the DTMF transceiver can be independently added to two different places: to the EOW line and to the output signal to the EOW phone.

G. Tone Generator

A sine wave generator is made by FPGA internal circuits and some external resistors. This tone generator can generate tones to the ringing signal amplifier or to the EOW phone in case of dial tone, busy tone etc.

H. V.11 Interface

Digital output of EOW is given out through v.11 interface via RJ45connectors.DS34LV87TM/AM26LV31 & S26LV32ATM are proposed to be used as differential driver and differential receiver.

I. Hard ware timer

Only one oscillator 16.384 MHz can be used. This will go to FPGA and FPGA will derive all other clocks for the system. Compact schematic diagram is shown in Figure 4.

III. EXTRACTION OF E1 BYTE FROM BY RECEIVING CALL

Figure 5 shows hardware block diagram for receive call from SDH network by E1 Byte.

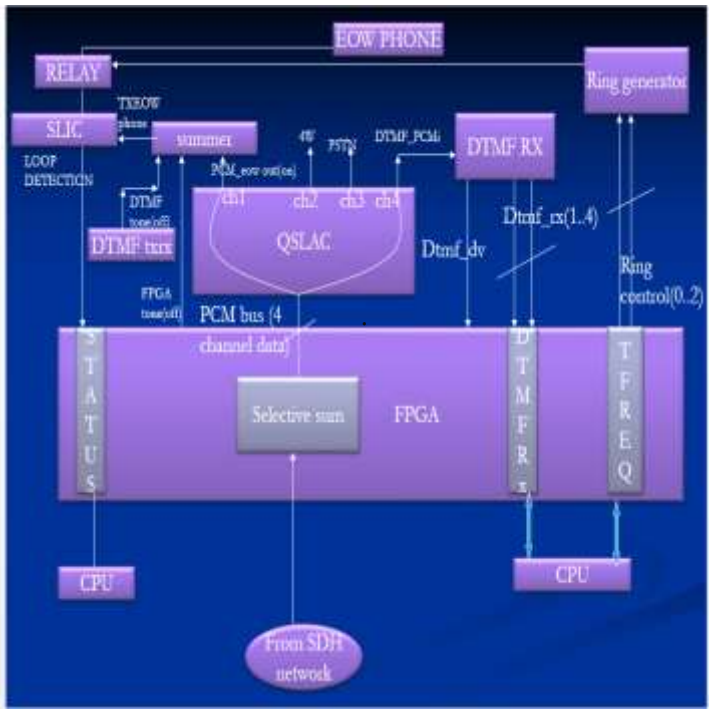

Fig. 5. Block diagram for receiving call from SDH network

Call from ring network means the data frame of SDH network enters into the FPGA via V.11 connector. FPGA decodes and extract data (E1-byte) from SDH frame. Then FPGA sum control unit sends data to CODEC. Data from CODEC is sent to DTMF receiver through one of the PCM channel .The DTMF receiver checks the data validity, if it is valid data then send to FPGA. If it is not valid data then it will simply discard the data. The valid data is read by CPU and compares the dial number. If the number matches, then CPU reads the HOOK condition of SLIC via FPGA. If the phone is in ON-HOOK condition, CPU activates ring generator control signal via FPGA. The relay is now active for ringing of phone. If the phone is in OFF-HOOK condition, FPGA sends busy acknowledgement signal to SDH network or it may be possible to send voice data to the phone from FPGA through CODEC and SLIC for conference call.

IV. INSERTION OF E1 BYTE BY TRANSMITTING CALL

Figure 6 shows hardware block diagram for transmit call to SDH network by E1 Byte. CPU reads the status of the phone via FPGA, if the phone is in OFF-HOOK condition, CPU set some register in FPGA to generate dial tone. Then the dial tone is transmitted to the phone through SLIC. The data is transmitted to DTMF transmitter to validate the data. If it is valid data, CPU will be interrupted via FPGA .CPU sends receive data to output as tone. If it is busy tone, FPGA generate and sends the busy tone to hand set via SLIC asking the caller to dial after sometime.

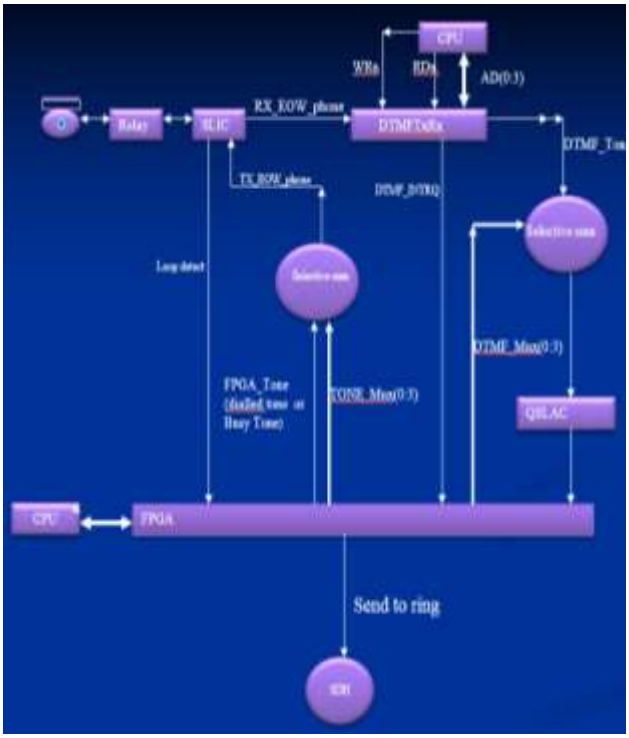

Fig. 6. Block diagram for sending call to SDH network

V. CONCLUSION

SONET/SDH networks are mature and have contributed much to the telecommunications and networking industry. In this paper it is shown that FPGA devices provide the ideal solution due to its embedded features within the transceiver blocks and its advanced architecture to meet the SONET/SDH specification. The attempt made in this paper may provide useful solutions for many programs using FPGA devices in future

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