

## Design & reduce the area of Combinational Circuits Using Reversible Cryptographer in Tanner Tools

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### Abstract

Reversible logic is the emerging field of research in the present era. The aim of this paper is to realize different types of combinational circuits like full-adder, full-subtractor, multiplexer, and comparator using reversible decoder circuits with minimum quantum cost. The reversible decoder designed using Fredkin gate with minimum Quantum cost. There are many reversible logic gates like Fredkin Gate, Feynman Gate, Double Feynman Gate, Peres Gate, Seynman Gate and many more. Reversible logic is defined as the logic in which the number output lines are equal to the number of input lines i.e., the n-input and k-output Boolean function  $F(X_1, X_2, X_3, \dots, X_n)$  (referred to as (n, k) function) is said to be reversible if and only if (i) n is equal to k and (ii) each input pattern is mapped uniquely to output pattern. The gate must run forward and backward that is the inputs can also be retrieved from outputs. When the device obeys these two conditions than the

second law of thermo-dynamics guarantees that it dissipates no heat. Fan-out and Feedback are Feedbacked in Logical Reversibility. Reversible Logic owns its applications in various fields which include Quantum Computing, Optical Computing, Nanotechnology, low power VLSI Etc., Reversible logic is gaining its own importance in recent years largely due to its property of low power consumption. The comparative study in terms of garbage outputs, Quantum Cost, numbers of gates are also presented. The Circuit has been implemented and simulated using Tanner tools v15.0 software.

**Keywords**-Quantum Cost, Reversible Gates, Garbage Outputs, Number of Gates.

**Abbreviations:** Feynman gate (FG), double feynman gate (DFG), toffoli gate (TG), fredkin gate (FDG), peres gate (PG), Thapliyal Ranganathan (TR), controlled NOT gate (CNOT).

## 1. Introduction

In present VLSI Technology, Power Consumption has become a very important factor for consideration. By using Reversible Decoder for designing Combinational circuits power consumption is reduced to an optimum when compared to conventional decoder based combinational circuits. Reversible Logic finds its own application in Quantum computing, Nano- technology, optical computing, computer graphics and low Power VLSI. Ralf Landauer [1] told that heat dissipation in circuits is not because of the process involved in the operation, but it is due to the bits that were erased during the process. He introduced that losing of a single bit in the circuit causes the smallest amount of heat in the computation which is equal to  $KT \ln 2$  joules where  $K$  is Boltzmann constant and  $T$  is Temperature. The amount of heat dissipated in simple circuits is very small but it becomes large in the complex circuits which imply propagation delay also. Later in 1973 C. H. Bennett [2] described that the Power dissipation due to the bit loss can be overcome if each and every computation in circuit was carried out in reversible manner. Quantum networks are designed of quantum logic gates. As each gate perform a unitary operation,  $KT \ln 2$  Joules energy dissipation wouldn't occur if the

computation is carried out in reversible manner. Thus computation done in reversible manner doesn't require erasing of bits. The amount of heat dissipated in the system holds a direct relationship to the number of bits erased or lost during the computation.

## 2. Concept

The Reversible Logic involves the use of Reversible Gates consists of the same number of inputs and outputs i.e., there should be one to one mapping between input vectors and output vectors. And they can be made to run backward direction also. Certain limitations are to be considered when designing circuits based on reversible logic (i) Fan out is not permitted in reversible logic and (ii) Feedback is also not permitted in reversible logic. In Reversible logic using outputs we can obtain full knowledge of inputs. Reversible logic conserves information. Some cost metrics like Garbage outputs, Number of gates, Quantum cost, constant inputs are used to estimate the performance of reversible circuits. Garbage outputs are the extra outputs which help to make inputs and outputs equal in order to maintain reversibility. They are kept alone without performing any operations. Number of gates count is not a good metric since more number of gates can be taken together to

form a new gate. Quantum Cost is the number of elementary or primitive gates needed to implement the gate. It is nothing but the number of reversible gates ( $1 \times 1$  or  $2 \times 2$ ) required to construct the circuit. Delay is one of the important cost metrics. A Reversible circuit design can be modeled as a sequence of discrete time slices and depth is summation of total time slices. In Digital Electronics the binary decoder is a combinational logic circuit that converts the binary integer value to the associated output pattern. Various proposals are given to design of combinational and sequential circuits in the undergoing research. In this paper, the design of different combinational circuits like binary comparator, Full adder, Full subtractor, multiplexer circuits using Reversible Decoder is proposed with optimum Quantum cost.

We formally define reversible gate, garbage output, delay in reversible circuit and quantum cost of reversible in reversible circuit. The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line.

### 3. Reversible logic gates

The basic reversible logic gates present in the literature are briefed below. The gates that are suitable for the design with optimum quantum cost can be selected.

#### a) NOT Gate:

The NOT GATE is the simple Reversible Logic gate. It is  $1 \times 1$  Reversible Logic Gate with the quantum cost zero. The Not gate simply shifts the complementary of the input to output as shown in the figure 1. It is the basic primitive gate which may involve in construction of reversible logic gate, thus owing its own importance in determining the quantum cost of designed Reversible logic gate.



INPUT	OUTPUT
A	P
0	1
1	0

Fig. 1 NOT gate & Truth table

#### b) Feynman Gate (FG)

Feynman gate is a  $2 \times 2$  reversible gate as shown in below figure 2. The Feynman gate is also called as CNOT gate i.e., controlled NOT gate. The Feynman gate is used to duplicate of the required outputs since Fan-out is not

allowed in reversible logic gates. The Quantum Cost of FG is 1. This is also the primitive gate owing its importance in determining quantum cost metric.

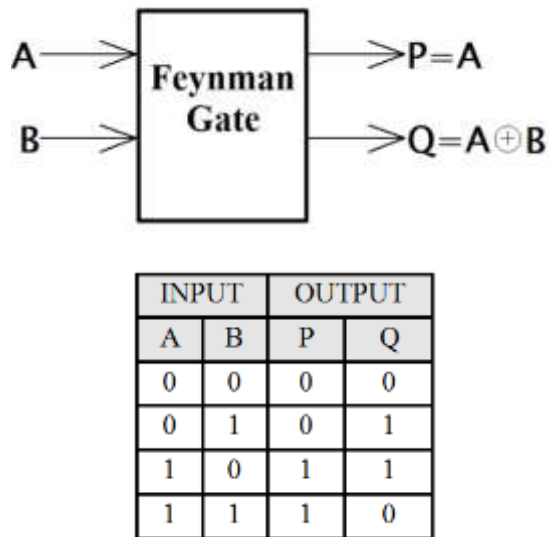


Fig. 2 FEYNMAN gate & Truth table

**c) Double Feynman Gate (DFG):**

Double Feynman Gate is a 3×3 reversible gate. The outputs are defined as shown in the below figure 3. The quantum cost of DFG is 2. This gate can also be used for duplicating outputs.

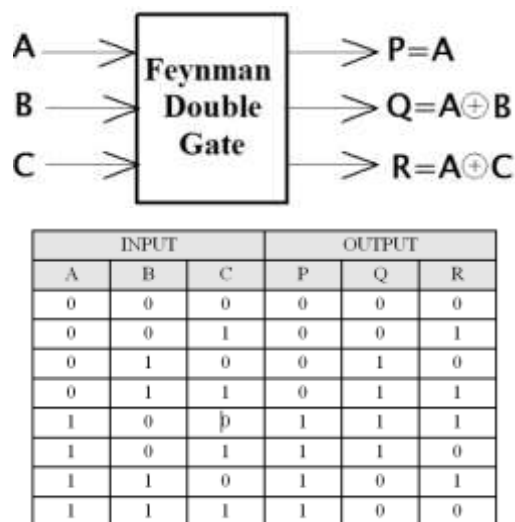


Fig. 3 DOUBLES FEYNMAN gate & Truth table

**d) Toffoli Gate (TG)**

Toffoli Gate is 3×3 reversible gate. The outputs are defined as shown in the below figure 4. The Quantum Cost of TG is 4.

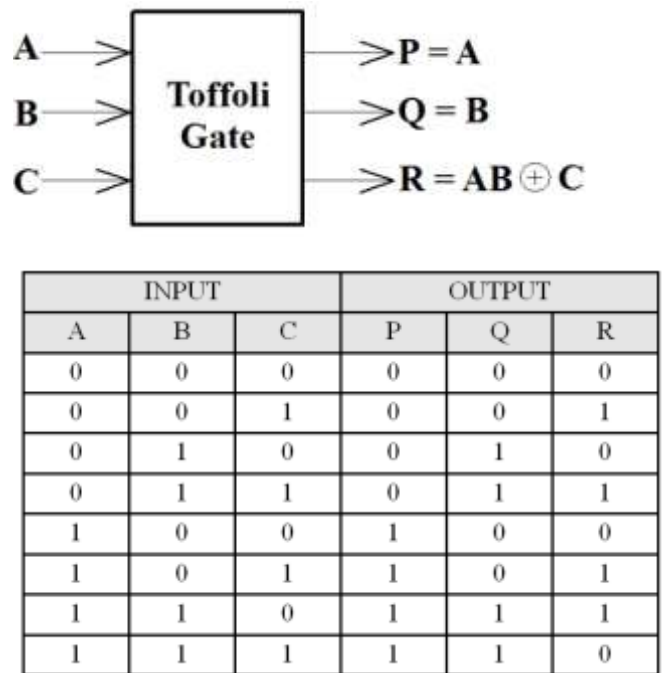
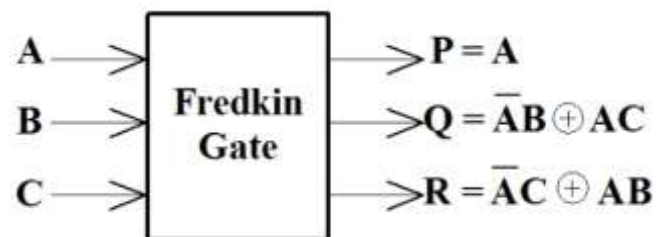


Fig.4 TOFFOLIC gate & Truth table

**e) Fredkin Gate (FDG)**

Fredkin Gate is a 3×3 reversible gate. The outputs are defined as shown in the below figure 5. The Quantum Cost of FDG is 5. This paper mainly surrounds around Fredkin gate.

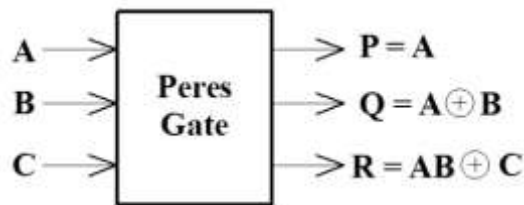


INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Fig.5 FREDKIN GATE & Truth table

**f) Peres Gate (PG)**

Peres Gate is a 3x3 reversible gate. The outputs are defined as shown in the below figure 6. The Quantum Cost of PG is 4.

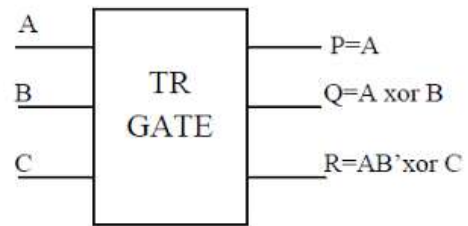


INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Fig.6 PERES GATE & Truth table

**g) TR gate**

TR (Thapliyal Ranganathan) Gate is a 3x3 reversible gate. The outputs are defined as shown in the below figure 7. The quantum cost of TRG gate is given by 4.

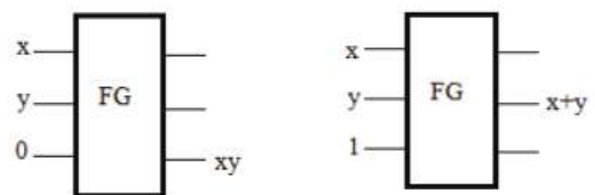


INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

Fig.7 TR GATE & Truth table

**4. Basic gates using reversible gates**

Considering our circuit requirements we need to design AND gate and OR gate using reversible gates. Here we used fredkin gate to design AND & OR gates as shown in figure 8. Importance is given to fredkin gate because it gives optimistic performance at less Quantum Cost for designing AND and OR gates.



INPUT			OUTPUT (AND-GATE)			OUTPUT (OR-GATE)		
A	B	C	AB	AC	Q	AC	AB	R
0	0	0/1	0	0	0	0	0	0
0	0	0/1	0	0	0	0	0	0
0	1	0/1	1	0	1	0	0	0
0	1	0/1	1	0	1	0	0	0
1	0	0/1	0	1	1	0	0	0
1	0	0/1	0	1	1	0	0	0
1	1	0/1	0	1	1	0	1	1
1	1	0/1	0	1	1	0	1	1

Fig.8 AND & OR Gate using fredkin gate

**5. Existing method**

The Design of Combinational and Sequential Circuits has been ongoing in research. Various proposals are given for the design of combinational circuits like adders, subtractors, multiplexers, decoders etc., in the existing method the author has given a novel design of 4x16 decoder whose Quantum Cost is less than the previous design. Replacing fredkin gates for designing 2x4 decoder reversible gates like peres gate, TR gate, NOT gate and CNOT gate are used as shown in figure9. The whole design is done using Fredkin, CNOT, Peres gates which give better Quantum Cost when compared to the other reversible Logic gates. The number of gates required to design 4x16 decoder are 18 in which there are 12 fredkin gates, one peres gate, one TR gate, one NOT gate and 3 CNOT gates. The sum of all the quantum costs of each gate gives total quantum cost of 4x16 decoder.

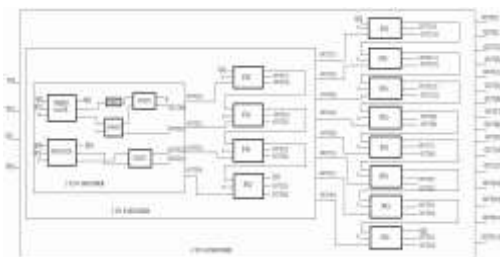


Fig 9: Block diagram of Reversible 4x16 decoder

**6. Proposed method**

Different Reversible Decoder circuits like 2x4, 3x8, 4x16 are designed using Fredkin Gates (mainly), Feynman gates and Peres gate. Some combinational circuits like comparator adder, subtractor, multiplexers etc., are designed using these decoders. The concept of duplicating a single output to required number of outputs using Feynman gate is introduced where Fan-out was not allowed in reversible computation. The Circuit has been implemented and simulated using Tannaer tools v15.0 software.

**7. Simulation results of proposed circuits**

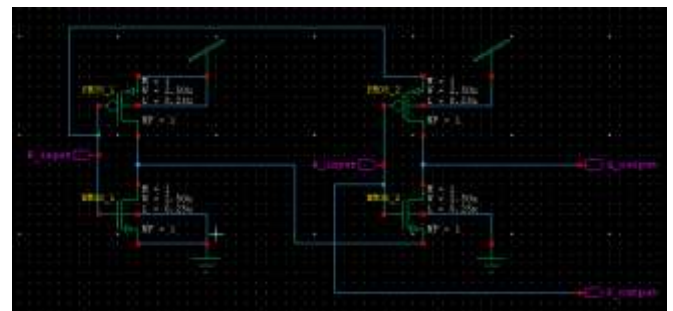


Fig.10 Schematic of feynmen gate

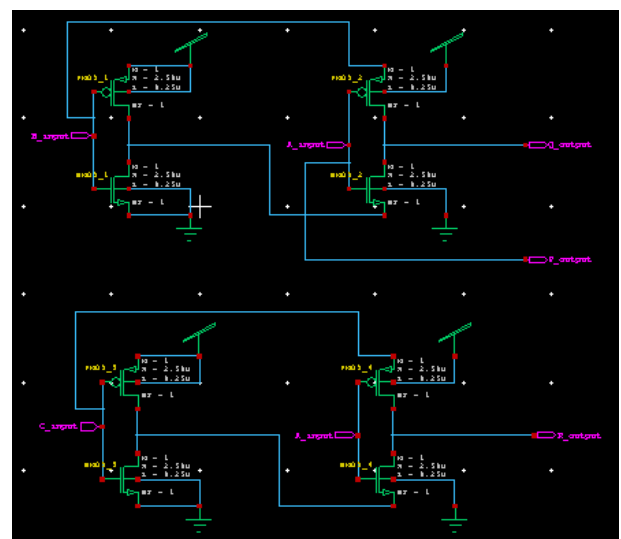


Fig.11 Schematic of double feynmen gate

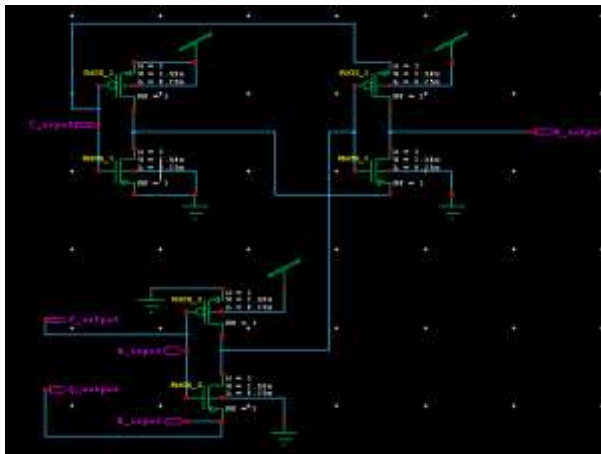


Fig.12 Schematic of toffolic gate

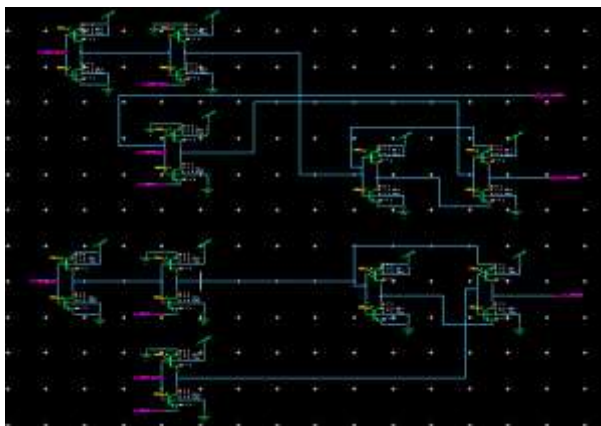


Fig.13 Schematic of fredkin gate

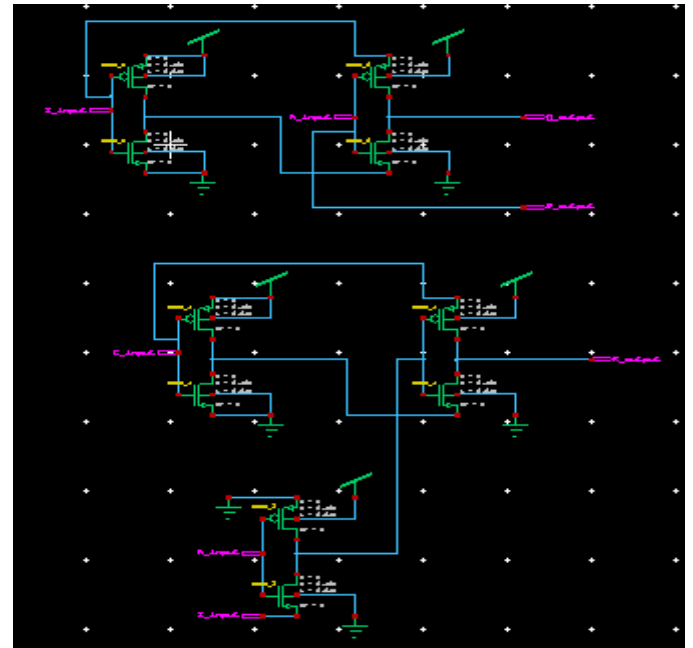


Fig.14 Schematic of peres gate

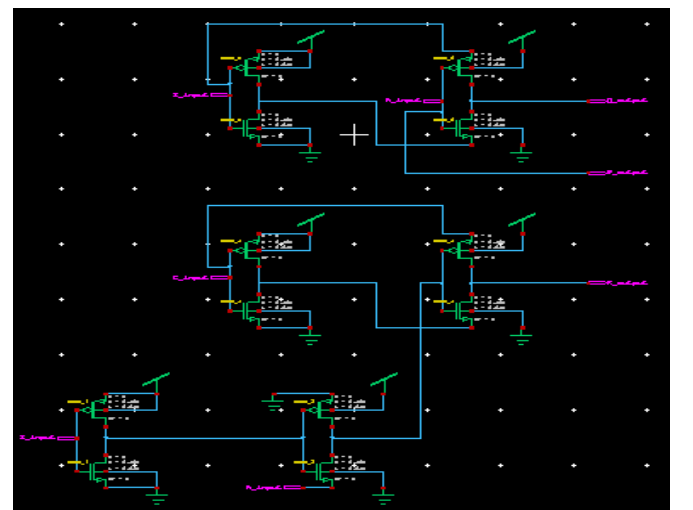


Fig.15 Schematic of TR gate

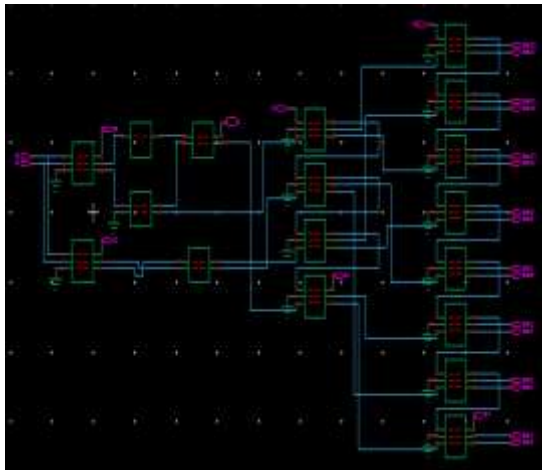


Fig.16 Schematic of 4:16 decoder

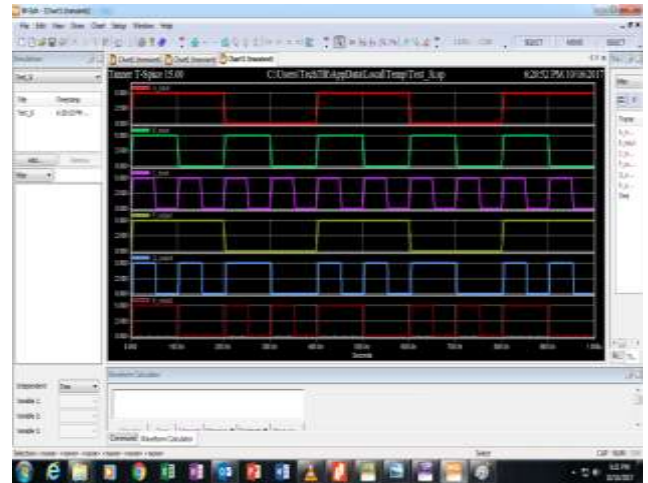


Fig.19 Schematic of fredkin gate waveform

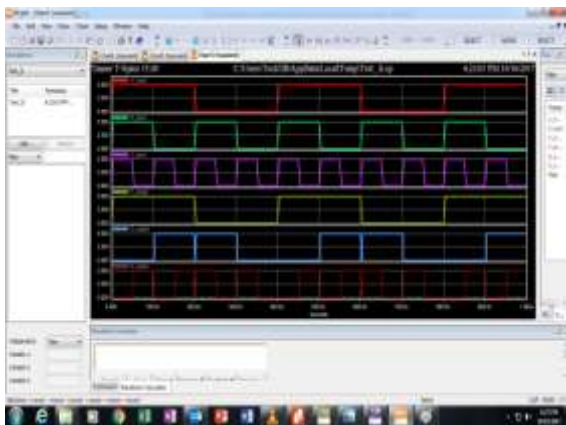


Fig.17 Schematic of double feynmen gate waveform

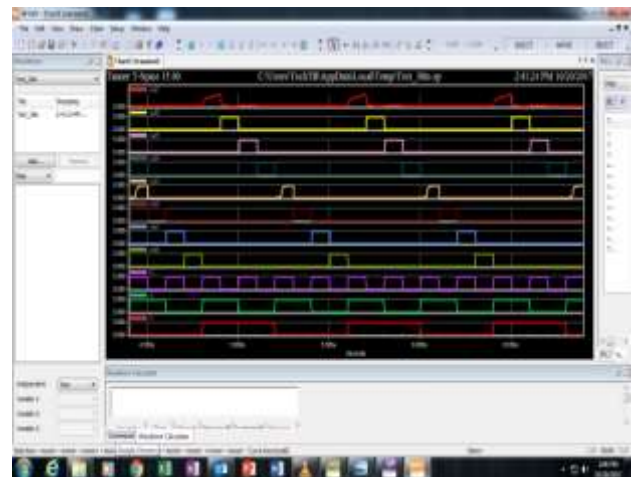


Fig.20 Schematic of 3:8 decoder gate waveform

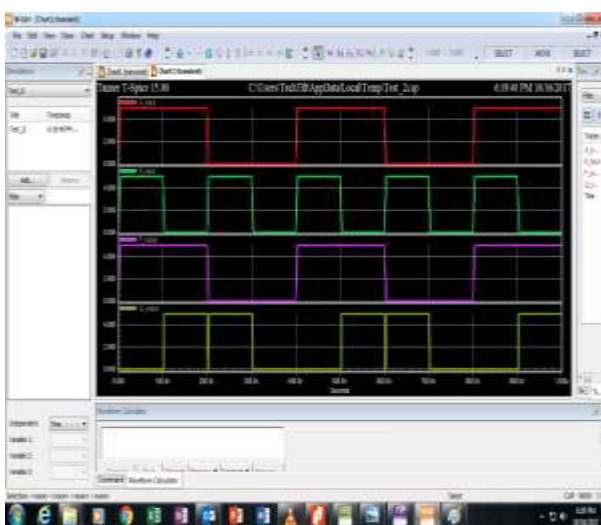


Fig.18 Schematic of feynmen gate waveform

It is clear from the above simulated output in figure 21 resembling stair case that different binary integer value is converted to associated pattern of outputs.



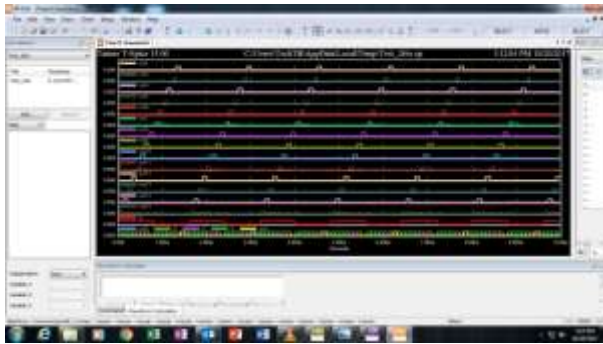


Fig.21 Schematic of 4:16 decoder gate waveform

Setup	0.41 seconds
DC operating point	0.27 seconds
Transient Analysis	16.96 seconds
Overhead	0.31 seconds
<b>Total</b>	<b>18.15 seconds</b>

Table II Power Results

MOSFETs	340
MOSFET geometries	6
Voltage sources	5
Sub circuit instances	35
Model Definitions	2
Computed Models	2
Independent nodes	170
Boundary nodes	6
Total nodes	176

Table I Device and node counts

Total Power from time	1e-009 to 1e-005
Average power consumed	1.095608e-001 watts
Max power	2.655809e-001 at time 1.20252e-006
Min power	8.167940e-002 at time 1.0025e-007
Parsing	0.20 seconds

### 8. Conclusion

In this paper, different combinational circuits like full adder, full subtractor, multiplexer, comparator circuits constructed using reversible decoder are designed. These circuits are designed for minimum quantum cost and minimum garbage outputs. The method proposed for designing the decoder circuit can be generalized. For example, a 3×8 decoder can be designed using a 2×4 decoder followed by 4 fredkin gates, Similarly a 4×16 decoder can be designed using 3×8 decoder followed by 8 fredkin gates .The concept of duplicating the single output to required number of outputs is utilized to overcome the fan-out limitation in reversible logic circuits as shown in table I & II. This method of designing combinational circuits helps to implement many digital circuits with better performance for minimum quantum cost.

## 9. References

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