Amplitude Modulation Technique in the field of Communication by Current Conveyor Circuit

Khushi Banerjee , Chittajit Sarkar
Electronics and Communication Engineering ,Asansol Engineering College

***Abstract*— This paper presents new amplitude modulator technique by using current conveyor which is more powerful component in analog domain. Four-MOS transistors switch and two-MOS transistors inverters, differential voltage current conveyor are required to design projected circuit. The planned circuit provides low-output and high-input impedance. Without buffer this can be attached to any load and suitable for integrated circuits since number of transistor is very less. A current conveyor based square wave generator supplies square pulse to control the switch. All simulation outcomes are based on the PSPICE simulator which confirms the validity of the proposed design.**

***Index terms*— AM modulator ,Differential voltage current conveyor, Second generation current conveyors (CCIIs)**

I. INTRODUCTION

It is found that second generation current conveyors (CCIIs) are very functional in several applications. These current conveyers provides larger dynamic range, greater linearity and high signal bandwidths compared to normal OPAMP based ones [1]–[7]. The differential voltage current conveyor (DVCC) was described in [5]. The DVCC has combined effects of the differential amplifier (DA) and the CCII. In case of amplitude modulation (AM), carrier signal with the frequency f_c modulates the amplitude of baseband signal with the frequency f_m where f_m is much smaller than f_c. Carrier signal may be sine wave or square wave. Square wave is basically used as carrier in Chopper modulator. The square wave carrier is used to slice the baseband signal in the chopper modulator as balanced one. Compared to Ring modulator circuit chopper modulator requires more filtering at the detector. Ring circuit is a double balanced modulator since it balances out both carrier and baseband signal. Ring chopper modulator by current conveyor has been described in Fig 1 [8]. Here the bias current of the current conveyor carries the carrier signal which makes chop signal probable through the bias current. The superiority of this circuit are: appropriate for integrated circuit realization, low power utilization.We suggest a new circuit that enhances the advantages of the circuit of [8] while reducing the disadvantages. The projected circuit consists of a DVCC, one inverter circuit and four MOS switches. The projected chopper modulators use 18 MOS transistors while the planned rectifier in [8] uses 43 MOS transistors; The anticipated rectifier will use smaller chip area than the previous one.

Fig. 2 shows the symbol of the DVCC. The CMOS implementation for DVCC can be shown in Fig.3.The matrix equation characterizes port relations. The MOS switches M_{S1}–M_{S4} and M_{S2}–M_{S3} are controlled by the square wave carrier voltage V_C and the square wave carrier voltage $-V_C$ respectively.There is a big resemblance of output between the new AM chopper modulator and the conventional sine wave carrier based AM modulator. It implies that the carrier frequency and output frequency are equal and also the output amplitude follows the baseband amplitude. This paper is organized in the following way :

Section-II describes the circuit diagram.The simulation results are described in section-III.The projected square wave generator is described in section IV followed by concluding remarks in section V.

II. CIRCUIT DESCRIPTION

In order to obtain these, VDC is used. Two signals will be shifted up with an offset higher than V_B peak to move these signal as the upper and lower envelopes of the whole AM signal. The fixed voltage VDC basically controls this shifting, i.e., VDC controls the modulation index. The provision of V_B peak will be used to circumvent the over-modulation .Consequently, AM chopper modulator can be found by $V_{DC} > V_B$(peak) and V_C and $-V_C$ mark that V_{Y1} and V_{Y2} consecutively work at the carrier rate, the output (V_X) of the planned circuit follows the envelopes of the AM signal sliced at the carrier rate. That is the AM chopper output. The proposed requires an adder circuit for adding DC voltage (V_{DC}) and baseband signal (V_B) (Fig. 4(c)). Here V_{DC} and V_B can be openly cascaded. For IC, an additional DVCC is used for the adder circuit. It can achieve by modifying the DVCC in Fig. 3 by floating the gate M2 to obtain additional plus type input (Y3). The voltages V_{DC} and V_B are applied to Y1 and Y3, respectively, and the minus type input (Y2) is attached to ground.

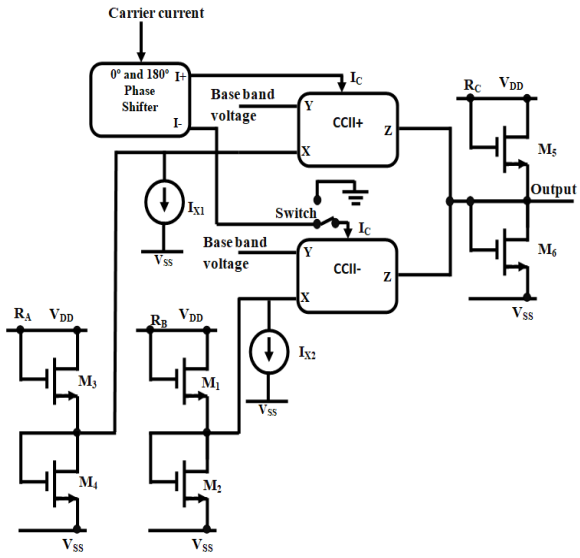

Fig.1 Modulator projected by Monpapassorn [8]

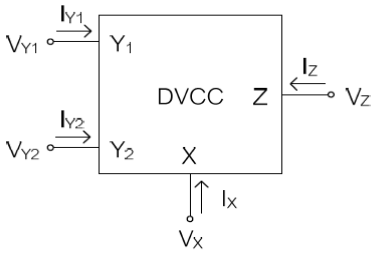

Fig.2 Symbolic representation of DVCC

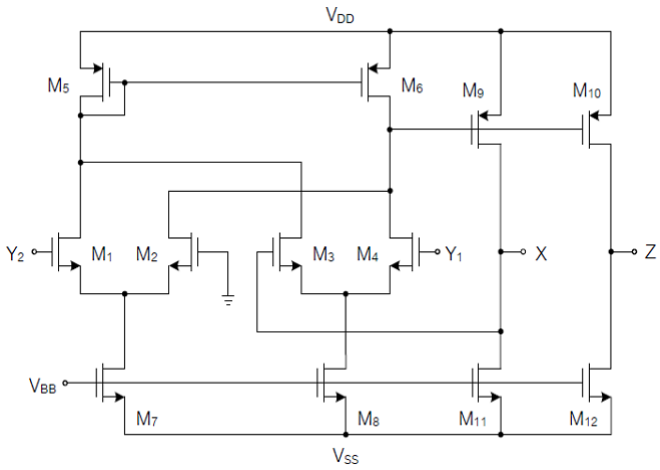

Fig .3 CMOS implementation of DVCC

$$\begin{pmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_Z \end{pmatrix} = \begin{pmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{pmatrix}$$

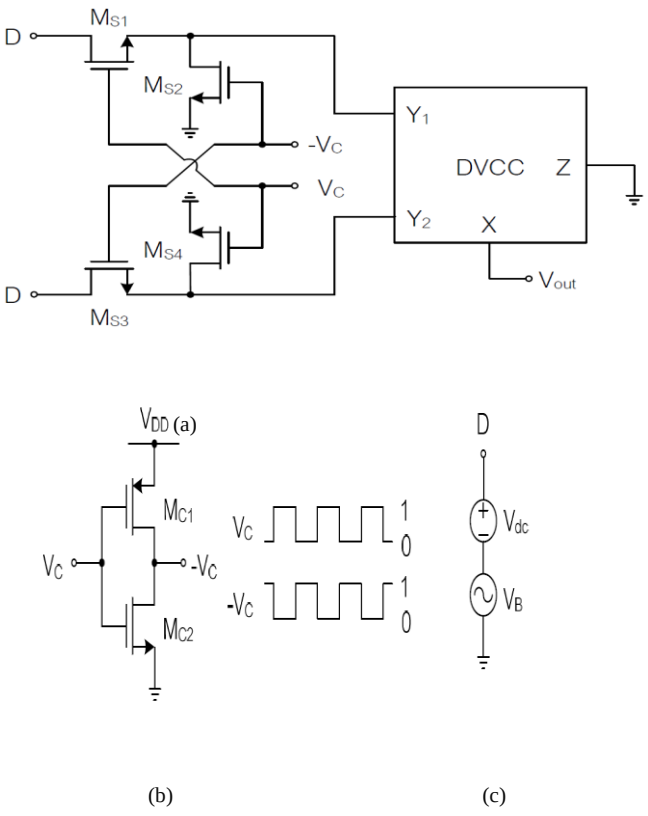

Fig 4. (a)Proposed chopper modulators, (b) MOS inverter and (c) adder voltages between V_{dc} and V_B.

III. SIMULATION RESULTS

To verify the theoretical prediction of the proposed circuit, the proposed chopper modulator in Fig. 4 has been simulated using PSPICE simulation program. The transistor aspect ratios are listed in [9] and the supply voltages were V_{DD}=−V_{SS}= 2.5 V and the biasing voltage was V_{BB}=-1.7 V. The aspect ratios of the transistors in Fig. 4 used are W/L = 2µm/1µm for M_{S1} to M_{S4},W/L = 8µm/1µm for M_{C1} and W/L = 20µm/1µm for M_{C2}.Applying the 200 m Vpeak of 10 kHz sine wave at V_B, the 1.5 V of 100 kHz square wave at V_C of the proposed circuit and V_{DC}= 0.25 V, the output position, the output waveform of AM chopper modulator can be shown in Fig. 7. These show the relations of square wave carriers, sine wave basebands and chopper modulator outputs that correspond to the theory. For simulation purpose, the operation of the chopper modulators can be understood by using simple carrier frequencies and baseband .The square

wave is taken from current conveyor based square wave generator.

IV. PROPOSED SQUARE WAVE GENERATOR

The DCCII [10]-[14] representation of inputs and outputs with corresponding current direction is shown in Figure.5. DCCII is a four terminal device among Y, X_P and X_N drives, input and the remaining Z terminal serve as output. The current differencing is the important property of DCCII , which is replicated across Z for the input current flowing across X_P and X_N. In addition, it deals a high input impedance which shows a vital role in the voltage cascading uses, The voltage applied through Y terminal is being copied to the other input terminals of X_P and X_N.

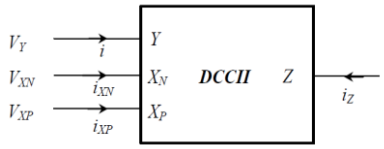

Fig.5 DCCII representation of inputs and outputs with corresponding current direction

$$\begin{bmatrix} V_{XN} \\ V_{XP} \\ i_Z \\ i_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{XP} \\ i_{XN} \\ V_Y \end{bmatrix}$$

The hybrid matrix of input and out terminal relation to ideal parameter consideration is presented in above .The proposed square wave generator with single DCCII, two resistors and a grounded capacitor is shown in Figure 6.

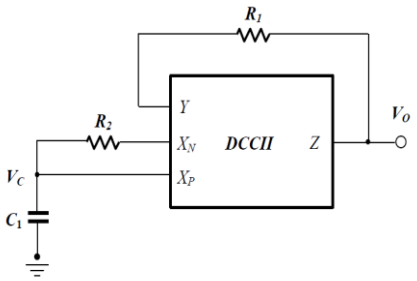

Fig.6 The proposed square wave generator with single DCCII

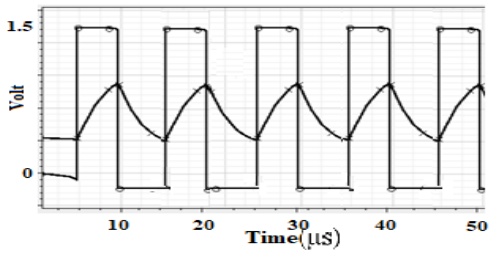

Fig.7 Square wave generator output

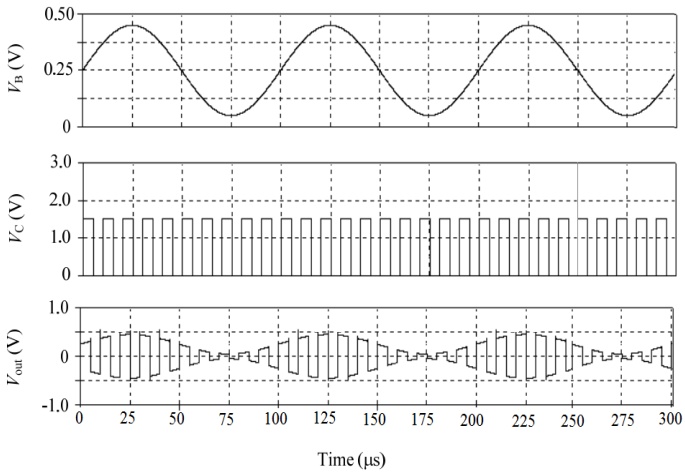

Fig.8 Operation of proposed modulator output

V. CONCLUDING REMARKS

In this manuscript, DVCC based AM chopper modulator has been presented.There are various advangtages of the proposed chopper modulators such as - simple for IC fabrication, less component count and simple to defend the over-modulation .The proposed chopper modulators are suitable for electronic communication system design.

REFERENCES

[1] Smith, K., Sedra, A. The current-conveyor - a new circuit building block. *IEEE Proceeding*, 1968, vol. 56, p. 1368–1369.

[2]Sedra, A., Smith, K. A second-generation current-conveyor and its applications. *IEEE Transactions on Circuit Theory*, 1970,vol. CT-17, p. 132–134.

[3]Fabre, A., Saaid, O., Wiest, F., Boucheron, C. Current controlled bandpass filter based on translinear conveyors.*Electronics Letters*, 1995, vol. 31, p. 1727–1728.
[4] A. Sallem, M. Fakhfakh, E. Tlelo-Cuautle, and M. Loulou, "Multi-objective simulation-based optimization for the optimal design of analog circuits," International Conference on Microelectronics (ICM), (2011), 1–4.
[5] Pal, K. Modified current conveyors and their application. *Microelectronic Journal*, 1986, vol. 20, p. 37–40.
[6] Elwan, H. O., Soliman, A. M. Novel CMOS differential voltage current conveyor and its applications. *IEE Proceeding of Circuits Devices and System*, 1997, vol. 144, p. 195–200.
[7] Pearson, J. E. *Basic Communication Theory*. UK: Prentice Hall, 1992.
[8] Monpapassorn, A. Chopper modulators using current conveyor analogue switches. *Analog Integrated Circuits and Signal Processing*, 2005, vol. 45, p. 155–162.
[9] Kumngern, M., Dejhan, K. DDCC-based quadrature oscillator with grounded capacitors and resistors. *Active and Passive Electronic Components*, 2009, doi: 10.115/2009/987304.
[10]A. Ahmet, and Y. Erkan, "Modified DVCC Based Quadrature Oscillator and Lossless Grounded Inductor Simulator Using Grounded Capacitor(s)," AEUInternational Journal of Electronics and Communications, (2017), 76, 86–96.
[11] A.D. Grasso, D. Marano, G. Palumbo, and S. Pennisi, "Analytical comparison of reversednested Miller frequency compensation techniques," Int. J. Circuit Theor. Appl., (2010), 38(7), 709–737.
[12]A.D. Marcellis, D.C. Claudia, F. Ferri, and V. Stornelli, "A CCII-based wide frequency range square waveform generator," International Journal of Circuit Theory and Applications, (2013), 41(1), 1–13.
[13] A. Emre, K. Pal, N. Herencsar, and B. Metin, "Design of Novel CMOS DCCII with Reduced Parasitics and its All-Pass Filter Applications," Elektronika ir Elektrotechnika, (2016), 22(6), 46–50.
[14] A. Kumar, and S.K. Paul, "Cascadable voltage-mode all-pass filter with single DXCCII and grounded capacitor," 2016 International Conference on 92 Microelectronics, Computing and Communications (MicroCom), Kharagpur, INDIA, (2016), 1–4.

AUTHORS

Khushi Banerjee, M.Tech,Ph.D pursuing
Assistant Professor, Asansol Engineering College.
Email address: bkhushi@gmail.com;

Dr.Chittajit Sarkar, Ph.D (Tech.)
Associate Professor, Asansol Engineering College.
Email address: chittajit_sarkar@yahoo.co.in;
chittajit.sarkar.in@ieee.org